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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,493	08/28/2003	Lukas Doerrer	1406/163	6981

25297 7590 05/19/2005

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SUITE 1400
DURHAM, NC 27707

EXAMINER	
YOUNG, BRIAN K	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,493	DOERRER ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4-8,10 and 12-18* is/are rejected.

7)☒ Claim(s) *3,9, and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claim 5 is objected to because of the following informalities: claim 5 recites "the adder" was has no antecedent basis in the claim. Appropriate correction is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 2,4-8,10, and 12-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Heikkila et al.

Heikkila et al disclose (fig.1) a quantizer for a multi-stage sigma delta modulator comprising at least one preliminary stage (H1), the quantizer quantizing an input signal (Ain) present at it in accordance with at least one threshold signal and outputting it as a result value at a digital result output (DOUT), wherein the quantizer has a number of comparators (H1-HS) corresponding to the number of threshold signals which compare the input signal with the respective threshold signal, the threshold signal being reduced or increased by a correction voltage (+Vref -Vref) or a correction current, the correction voltage or correction current being generated in accordance the out put signal.

Heikkila et al recite (col. 3, lns.15-31) In FIG. 1, a comparator 25 monitors the output voltage/digital value of the last integrator H.sub.5 and compares it to a predetermined ***threshold*** value REF. When the ***threshold*** value is exceeded, the comparator 25 outputs a control signal 26, which changes the coefficients b2 and b3 of the scaling

means 22 and 23. The comparator 25 may also monitor the output of another integrator H.sub.1, H.sub.2 or H.sub.3. The modulator may also comprise several comparators 25 so that the outputs of several integrators can be monitored simultaneously. In A/D converters integrators are analogous, and the comparator 25 is usually also analog then. In D/A converters the integrators are digital, in which case the comparator 25 monitors whether an integrator overflows or whether the digital output word of the integrator exceeds a predetermined digital ***threshold*** value.

FIG. 5 shows a feed forward modulator configuration. The modulator comprises the integrator stages H.sub.1, H.sub.2, H.sub.3 and H.sub.4 connected in series. In a subtractor means 51, a feedback signal from the output of the modulator is subtracted from the input signal A.sub.IN of the modulator, and the difference is applied to the first integrator stage. The output of the integrator H.sub.1 is applied to the integrator H.sub.2, the output of the integrator H.sub.2 to the integrator H.sub.3, and the output of the integrator H.sub.3 to the integrator H.sub.4. The outputs of the integrators H.sub.1, H.sub.2, H.sub.3 and H.sub.4 are also connected to a summing means 56 through scaling means 52, 53, 54 and 55, respectively. The scaling coefficients of the scaling means 52, 53, 54 and 55 are a1, a2, a3 and a4, respectively. The summing means 56 supplies a sum signal to a quantizer 57, which provides a digital output signal D.sub.OUT, which is the output signal of the modulator. The signal D.sub.OUT is also connected to a scaling means 58, which provides the aforementioned feedback signal by scaling the signal D.sub.OUT by coefficient b1. The modulator also comprises a

stabilization circuit according to the invention, consisting of a comparator 59 and an adjustable scaling means 58. The comparator 59 compares the output signal of the integrator H.sub.4 to a predetermined ***threshold*** value. When this ***threshold*** value is exceeded, the modulator is concluded to be in an unstable mode, and the comparator 59 supplies a control signal 60, which causes the adjustable scaling means 58 to change the feedback coefficient b1. The adjustable scaling means 58 may be realized in the same way as the scaling means 22 in FIG. 2. The unstable mode of the modulator may also be detected in different ways described in connection with FIGS. 1 to 4.

The modulator comprises a switching means 20 which ***selects*** one of reference voltages +V.sub.ref and -V.sub.ref as the feedback signal on the basis of the mode of the digital output signal D.sub.OUT of the quantizer 15 (and of the entire modulator). Scaling means 21, 22, 23 and 24 scale the selected feedback signal by the aforementioned feedback coefficients b1, b2, b3 and b4. The coefficients may be for example the following: b1=1, b2=4, b3=16, and b4=64.

In this way selector 20 functions as a DAC.

4. Claims 3,9, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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